Implementation of Carrier Frequency Offset and IQ Imbalance Compensation in OFDM Systems

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Abstract—**This work presents synchronization and *IQ* imbalance compensation circuits for OFDM WLAN receivers. A CORDIC-based Sinusoid Iteration Generator (CSIG) is also proposed for CFO estimation in wireless communication. Except for the main effect from the multi-path, some non-ideal effects from imperfect hardware design, such as the *IQ* imbalance from direct conversion in RF front-end, should also be considered. An *IQ* imbalance compensation circuit in IEEE 802.11(a) baseband receiver is then proposed. A low-complexity time-domain compensation algorithm is adopted to replace the traditional high-order equalizer. The system is implemented and verified by TSMC 0.18um COMS 1p6m technology.**[1]

I. Introduction

WIRELESS local area network (WLAN) access has been rapidly deployed and extended worldwide in recent years. The development of wireless systems for high data-rate transmission has become an important field of research. Orthogonal frequency division multiplexing (OFDM) based WLAN technology has received attention due to its high data rate. OFDM is an effective and spectrally efficient signaling technique for communication over frequency selective fading channel. Unfortunately, OFDM is also sensitive to non-ideal front-end effect and non-perfect synchronization, which result in *IQ* imbalance and carrier frequency offset (CFO) errors, thus significantly degrading the communication receiver's performance. Various studies have considered IQ imbalances and CFO separately [1]–[3].

The increase in required transmission speed of the WLANs means that a higher-order modulation of quadrature amplitude modulation (QAM) is needed to improve the data rate. Thus, the *IQ* imbalance causes a severe degradation of demodulation performance. *IQ* imbalance results from a nonideal front-end component due to the power imbalance or the non-orthogonality between inphase (*I*) and quadrature (*Q*) branches. The digital algorithms and implementations are required to compensate *IQ* imbalance and to improve demodulation accuracy. Therefore, a very low-complexity hardware architecture is adopted to estimate and correct *IQ* imbalance.

Several methods for compensating *IQ* imbalance in OFDM transmission were presented [4]–[6]. Held *et al.* [4] presented a non-adaptive time-domain method for estimation and correction of *IQ* imbalance in OFDM WLAN receivers. Tubbax *et al.* [5] presented a compensation method that eliminates the *IQ* imbalance based on one OFDM symbol. Their method performs well in the presence of phase noise. Schuchert *et al.* [6] applied a frequency-domain method that targets DVB with an adaptive equalizer. The proposed of low-complexity digital *IQ* imbalance and CFO compensation hardware architectures are practically implemented for OFDM receivers to eliminate distortions and carrier offset in the time domain.

This paper is organized as follows. The system block diagram of the OFDM baseband receiver is described in Section II. The low-complexity schemes of carrier frequency synchronization and *IQ* imbalance are described in Section III and IV, respectively. Implementation results are shown in Section V. Finally, Section VI concludes this investigation.

II. System Block Diagram

Synchronization is an essential task to receive transmitted data reliably in a digital communication system [7]. The PLCP preamble in the IEEE 802.11a standard is designed for synchronization [8]. The first seven short preamble symbols are used for automatic gain control (AGC) and frame detection. The last three short preamble symbols are used for timing estimation and coarse CFO estimation. Channel estimation and fine CFO estimation are then performed by the two long preamble symbols. In the proposed system, AGC and clock synchronization are performed before frame detection, and the received signal *r(t)* is assumed to be affected by additive white gaussian noise (AWGN), Rayleigh fading, frequency offset and *IQ* imbalance effect.

Figure 1 shows the overview of IEEE 802.11a baseband transmission, including the transmitter and receiver. The transmitter comprises the following components: a scrambler to scramble the transmit data; a convolutional

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encoder to reduce the number of transmitted bits and increase the coding rate; an interleaver to prevent consecutive errors; mapper to modulate the subcarriers, and a windowing system. The receiver works in the opposite direction to the transmitter. Moreover, some synchronization circuits resist the channel effect in the receiver. This study focuses on designing and implementing the synchronization circuit with IQ compensation in the receiver. The architecture in Fig. 1 is adopted to simulate and implement CFO and IQ imbalance compensation. The blocks with dotted line denote the channel effects. The CFO and IQ imbalance compensation block is implemented in time-domain to increase demodulation performance.

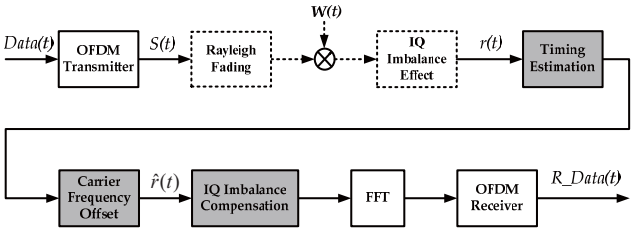

Fig. 1 System block diagram of OFDM-based basedband receiver.

III. CFO AND *IQ* IMBALANCE

A. Carrier Frequency Synchronization

Assume that the transmission is under a slow fading channel such that the short symbol is similar. A correlator that takes Maximum Likelihood Estimation (MLE) for CFO is adopted [9]. The IEEE 802.11a uses the last three short symbols for coarse CFO estimation. The following algorithm can use any successive three short symbols after AGC can be used.

To reduce the estimated coarse CFO $\hat{\xi}$ hardware implementation cost, an adopted equation given by Peng and Wen [9] can be modified into

$$\hat{\xi} = \frac{1}{2\pi N_s}\arg\left(\frac{\sum_{n=0}^{15}\left[Y_s(k,n)Y_s^*(k+1,n)+Y_s(k+1,n)Y_s^*(k+2,n)\right]}{2}\right) \quad (1)$$

where arg(.) denotes the argument and $Y_s(k,n)$ denote the received noisy output through the channel at nth sample of kth symbol. Equation (1) clearly reveals that the delay and correlate architecture of autocorrelation is reused here besides frame detection. It is suitable for hardware design. The fine CFO estimation is similar to the derivation process of the coarse CFO with N_L =64 indicating long preamble signals, yielding

$$\hat{\xi}_{fine} = \frac{1}{2\pi N_L}\arg\left[\sum_{n=0}^{N_L-1}\hat{Y}_L(0,n)\cdot\hat{Y}_L^*(1,n)\right] \quad (2)$$

where $\hat{Y}_L(m,n) = Y_L(m,n)\cdot\exp\left(-j2\pi(n+N_L)\hat{\xi}\right)$ with m=0,1.

The phase shift increase in size, since the OFDM symbols are received continuously. Small-phase rotation caused by CFO still occurs after OFDM symbols passing through FFT. According to each OFDM symbol, four pilot subcarriers exist, with the value inserted into the 48 data subcarriers. The rotated phase can be obtained

$$\hat{\phi} = \arg\left(\sum_{k=-21,-7,7,21}\left(\hat{Y}_{l,k}P_{l,k}^*\right)\right) \quad (3)$$

where $\hat{Y}_{l,k}$ denotes signal k of symbol l, and $P_{l,k}$ denotes the pilot value at frequency subcarrier k. The received data are retrieved by the frequency and phase synchronization, given by

$$\hat{r}_k = r_k\cdot\exp(-j2\pi(\hat{\xi}+\hat{\xi}_{fine})k+\hat{\phi}) \quad (4)$$

where k=0, 1, 2, …, and r_k denotes the complex signals beginning from long symbols.

B. IQ Imbalance Compensation

IQ imbalance can be characterized by two parameters, the amplitude imbalance K as a power mismatch between the I and Q branches, and the phase imbalance φ_{err} yielding an orthogonality mismatch between the I and Q branches. A popular model for an *IQ* imbalance impaired signal $s = s_I + js_Q$ is given by

$$\begin{bmatrix}s_I[k]\\ s_Q[k]\end{bmatrix} = \begin{bmatrix}K_I & 0\\ -K_Q\cdot\sin\varphi_{err} & K_Q\cdot\cos\varphi_{err}\end{bmatrix}\cdot\begin{bmatrix}s_I'[k]\\ s_Q'[k]\end{bmatrix} \quad (5)$$

where s'_I and s'_Q denote the components of the unimpaired signal. The amplitude imbalance K is represented by the two symmetrical factors K_I and K_Q, while the phase imbalance is given by φ_{err}.

The *IQ* imbalance compensation circuit adopts a time-domain compensation algorithm to minimize complexity and maintain stable performance [4]. A long preamble of L=64 estimated *IQ* imbalance compensation parameters is adopted herein. Equation (6) is employed to derive the amplitude (K_{est}) and phase (P_{est}) of the *IQ* imbalance parameters. Equation (7) is employed to compensate the amplitude and phase imbalances.

$$K_{est} = \sqrt{\frac{\sum_{k=1}^{L}s_Q^2[k]}{\sum_{k=1}^{L}s_I^2[k]}}, \qquad P_{est} = \frac{\sum_{k=1}^{L}\left(s_I[k]\cdot s_Q[k]\right)}{\sum_{k=1}^{L}s_I^2[k]} \quad (6)$$

$$\text{amplitude}: \begin{cases} w_I[k] = S_I[k] \\ w_Q[k] = S_Q[k] / K_{est} \end{cases}$$
$$\text{phase}: \begin{cases} w_I[k] = S_I[k] \\ w_Q[k] = \dfrac{1}{\sqrt{1-P_{est}^2}} \cdot S_Q[k] - P_{est} \cdot S_I[k] \end{cases} \quad (7)$$

As Fig. 2 shows, the 64-QAM constellation is obtained after CFO and *IQ* imbalance compensation with an amplitude imbalance of K =3dB, SNR=25, and a phase imbalance φ_{err} =10°. Figure 3 compares the bit error rate (BER) of demodulating signals with and without *IQ* imbalance correction in the AWGN channel. *IQ* imbalance is not apparent in lower-order QAM modulation. However, in higher-order QAM modulation, it will become serious interference.

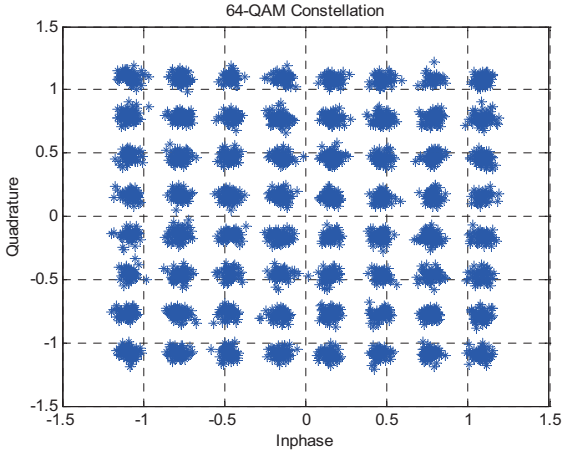

Fig. 2 64-QAM constellation compensation by CFO and *IQ* imbalance compensation.

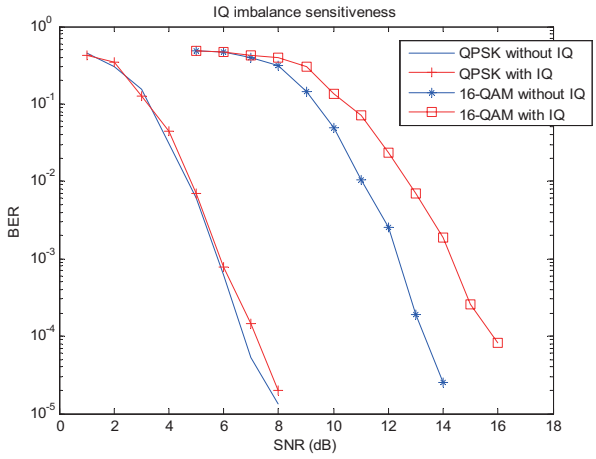

Fig. 3 Performance comparison with and without IQ imbalance effect.

IV. Implementation Results

A. CFO Compensation

CFO estimation comprises coarse and fine CFO estimation. Coarse CFO estimation employs the real and imaginary parts of output values of the autocorrelation during the short preamble. To improve the precision, fine CFO estimation is used as in coarse CFO estimation, but is adopted during the long preamble. The architecture of coarse and fine CFO estimation can be combined as depicted in Fig. 4. To reduce the hardware area, the coarse and fine CFO estimation can adopt the same divisor, because they work at different times. The receiver performs the first rotation and the second rotation for coarse CFO estimation and fine CFO estimation respectively.

The upper part of Fig. 4 is an architecture of coarse CFO estimation. Once the real and image parts of output values of the autocorrelation are obtained, the real part is given by I, and the image part is given by Q. Thus, the tangent value is computed by dividing Q/I. The rotated angle of CFO is calculated as $\theta = tan^{-1}(Q/I)$. An arctangent table is needed to find the angle. If the angle (θ) is smaller than radian 0.5, then the quotient is obtained as $Q/I = tan\theta \fallingdotseq \theta$.

The Coordinate Rotation Digital Computer (CORDIC) architecture is adopted to rotate the frequency offset vector to the front-end of the CORDIC-based sinusoid iteration generator (CSIG), as shown in Fig. 5. If the initial vector is on the real axis, then the real axis signal X_0 = 1, and the imaginary axis signal Y_0 = 0. The auxiliary computing angle Z_0 is a phase rotation that can be estimated by the autocorrelation. The stage controller is influenced by the signal Z_{out}, and controls the shifters and the $\tan^{-1}$ table. The values of $\sin\theta$ and $\cos\theta$ are given as constants. The modified equations are given as

$$\begin{aligned} S_{i+1} &= S_0 C_i + C_0 S_i \\ C_{i+1} &= C_0 C_i - S_0 S_i \end{aligned} \quad (8)$$

where $S_0 = \sin\theta$ and $C_0 = \cos\theta$. The sinusoid iteration architecture in Fig. 5 receives the real and imaginary signals from the CORDIC architecture. The stage controller starts the modified oscillation, and controls the iteration feedback computation. The last frequency rotated vectors ($\boldsymbol{S}_{i+1}$, $\boldsymbol{C}_{i+1}$) are calculated from the current rotated vectors ($\boldsymbol{S}_i$, $\boldsymbol{C}_i$) and the initial phase offset ($\boldsymbol{S}_0$, $\boldsymbol{C}_0$).

The architecture of fine CFO estimation resembles that of coarse CFO estimation, except that the depth of autocorrelation is sixty-four. Additionally, since the angle to be detected by fine CFO estimation is very small, the value of $\sin\theta$ can be viewed as θ, and the value of $\cos\theta$ equals 1. Restated, the architecture of fine CFO estimation does not need CORDIC to calculate the first rotated vector. The initial values in (8) thus become $S_0 = \theta$ and C_0=1.

B. IQ Imbalance Compensation

A received OFDM signal impaired by both amplitude and phase imbalance is compensated in two phases: performing amplitude imbalance estimation and compensation, and then performing phase imbalance estimation and compensation as given in (6) and (7). Figure 6 illustrates the foregoing

correction method of hardware structure for *IQ* imbalance compensation. The first step is to wait for the start trigger from the front-end signal when the long preamble symbol is detected. The parameter K_{est} is then calculated according to the amplitude estimation equation, and the amplitude compensation (I_A_ok and Q_A_ok) is obtained by Amplitude Corrector (A.C.). The parameter P_{est} can be calculated based on the phase estimation equation and the phase compensation, and the unimpaired signal (I_ok and Q_ok) can be attained through the Phase Corrector (P.C.). The shaded calculation circuit block in Fig. 6 can be reused by hardware combination for low cost. Table I lists the implementation results in terms of timing, area and power.

V. Conclusion

This work has presented the synchronization circuit for timing and CFO estimation and the *IQ* imbalance compensation circuit in an IEEE802.11a baseband receiver. A CSIG architecture for CFO estimation that can efficiently reduce the hardware cost is proposed for wireless systems. Moreover, a low complexity time-domain *IQ* compensation algorithm is adopted to implement the hardware architecture. This study uses system simulation to produce the test signals and verify the effectiveness of the compensation circuit through the cell-based design process. This architecture is implemented and verified by TSMC with 0.18 μm 1P6M CMOS technology for the 600 kHz frequency offset and *IQ* imbalance in a wireless system.

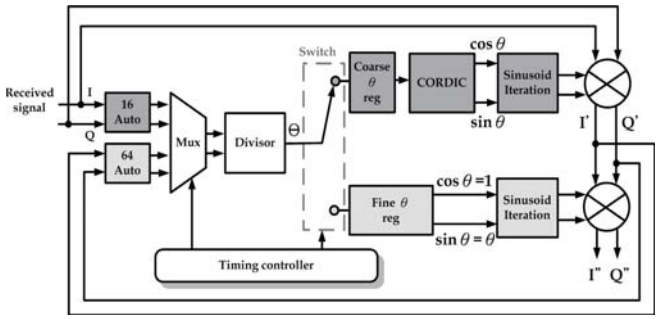

Fig. 4 Combinational circuit of fine and coarse CFO estimation.

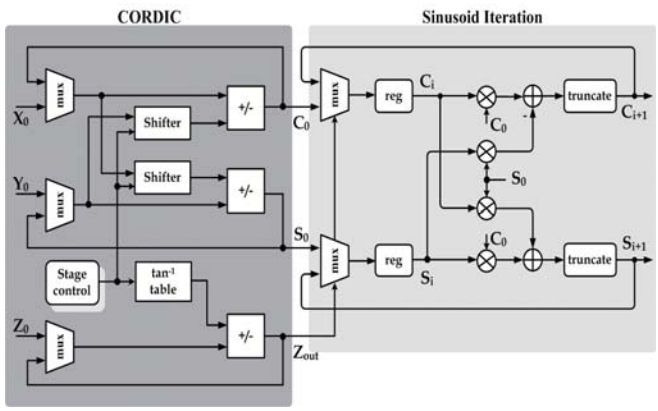

Fig. 5 The CSIG architecture.

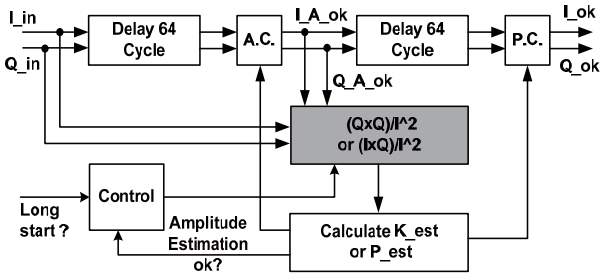

Fig. 6 The block diagram of IQ imbalance compensation circuit.

TABLE I
Performance of our Proposed Architecture

Technique	TSMC 0.18 1p6m
Operation Frequency	20MHz
Area	1.588mm^2
Gate Count	158853
Power	16.572mW

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